Gary M. Hoffman (*Pro Hac Vice*)
Kenneth W. Brothers (*Pro Hac Vice*)
DICKSTEIN SHAPIRO LLP
1825 Eye Street, NW
Washington, DC 20006-5403
Telephone: (202) 420-2200
Facsimile: (202) 420-22019

Edward A. Meilman (*Pro Hac Vice*)
DICKSTEIN SHAPIRO LLP
1177 Avenue of the Americas
New York, NY 10036-2714
Telephone: (212) 227-6500
Facsimile: (212) 227-6501

Jeffrey B. Demain, State Bar No. 126715
Jonathan Weissglass, State Bar No. 185008
ALTSHULER, BERZON, NUSSBAUM, RUBIN & DEMAIN
177 Post Street, Suite 300
San Francisco, CA 94108
Telephone: (415) 421-7151
Facsimile: (415) 362-8064

Attorneys for
RICOH COMPANY, LTD.

UNITED STATES DISTRICT COURT
NORTHERN DISTRICT OF CALIFORNIA
SAN FRANCISCO DIVISION

RICOH COMPANY, LTD., Plaintiff, vs. AEROFLEX INCORPORATED, et al., Defendants	**CASE NO. C-03-4669-MJJ (EMC)** **DECLARATION OF KENNETH BROTHERS IN SUPPORT OF RICOH'S REPLY IN SUPPORT OF RICOH'S MOTION FOR SUMMARY JUDGMENT ON AEROFLEX'S AFFIRMATIVE DEFENSE OF "AUTHORIZATION AND CONSENT"** Date: September 26, 2006 Time: 9:30 a.m. Courtroom: 11, 19th Floor Judge: Martin J. Jenkins

Kenneth W. Brothers declares as follows:

1. My name is Kenneth W. Brothers, an attorney with the law firm of Dickstein Shapiro LLP, counsel for Ricoh Company Limited. I am over the age of 21 and am competent to make this declaration. Based on my personal knowledge and information, I hereby declare to all the facts in this declaration.

2. In court filings between November 2005 and April 2006, and in several meet and confers at the end of May and early June 2006, Aeroflex's counsel repeatedly asserted that it was not relying upon any form of an implied authorization and consent defense and was only relying on express authorization and consent. I relied upon these statements in seeking discovery limited to express authorization and consent.

3. Attached hereto as Ex. 1 is a true and correct copy of my May 31, 2006 email to Denise De Mory summarizing the case law on implied authorization and consent.

4. Attached hereto as Ex. 2 is a true and correct copy of ITT Industries, Inc.'s May 15, 2006 objections to Ricoh's subpoena, which had been served upon ITT on May 9, 2006.

5. Attached hereto as Ex. 3 is a true and correct copy of a press release dated March 27, 2000, concerning the "0.6 micron GATE ARRAY FAMILY," found on Aeroflex's web site, printed September 8, 2006, available at http://www.ams.aeroflex.com/ProductFiles/News/06press.pdf (visited September 6-8, 2006).

6. Attached hereto as Ex. 4 is a true and correct copy of a December 2003 "Data Sheet" for the 0.6 micron "Gate Array Family" found on Aeroflex's web site, printed September 8, 2006. This document is available at http://www.ams.aeroflex.com/ProductFiles/DataSheets/ut06crhsrh.pdf (visited September 6-8, 2006). Aeroflex produced this document with bates numbers AF 179675 – AF179690 and inexplicably marked the document as "Confidential."

I declare under penalty of perjury under the laws of the United States of America that the foregoing is true and correct. Signed at Washington, D.C. on September 8, 2006.

September 8, 2006

/s/ Kenneth W. Brothers
Kenneth W. Brothers

EXHIBIT 1

Brothers, Kenneth

From: Brothers, Kenneth
Sent: Wednesday, May 31, 2006 9:18 PM
To: DeMory, Denise
Cc: 'Fink, Jacky'
Subject: Law regarding authorization and consent

Denise:

Following up on our conversation today, as a good faith showing, I forward the following information to you regarding the 1498 defense in hopes of persuading you to designate an Aeroflex witness on six sub-topics of topics 3 of Ricohs' May 4, 2006 notice for which you have refused to provide a designee. Section 1498 provides for "authorization and consent" to a contractor, but the statute is explicit that authorization and consent may be granted only by the Government, and not by the prime contractor: "For the purposes of this section, the use or manufacture of an invention described in and covered by a patent of the United States by a contractor, a subcontractor, or any person, firm, or corporation for the Government <u>and with the authorization or consent of the Government</u>, shall be construed as use or manufacture for the United States."

The Federal Procurement Regulation (FAR) provides for different types of consent that may be included in Government contracts. In the majority of government contracts, the FAR at 48 CFR § 27.201-2(a) and 48 CFR § 52.227-1 provides for inclusion of a "limited" authorization and consent clause, using language which grants the Government's authorization and consent, but only where (i) the patented invention is embodied in the structure or composition of an article accepted by the Government, or (ii) the patented invention is used in tools or methods whose use "necessarily results" from compliance with specifications in the Government contract or specific written instructions from the contracting officer. <u>See</u> FAR 52.227-1. Based upon our review of the prime contracts related to the Aeroflex products at issue, there is only a limited authorization and consent clause.

As such, in the case of infringement of a process patent, authorization and consent is only granted where the use of that process "necessarily results" from compliance with specifications in the Government contract or specific written instructions from the contracting officer. If the infringement was not necessary, then the Government has not given its authorization and consent. It makes no difference whether the infringement was done by a prime contractor or subcontractor, or whether a prime contractor gave specific instructions to a subcontractor.

The leading case for the proposition that unnecessary infringement does not receive "authorization and consent" under the standard FAR clause (the same as it exists today) is <u>Carrier Corp. v. United States</u>, 208 Ct. Cl. 678 (1976). In that case, the Government argued that "since neither the contract specifications nor any specific written instructions from the contracting officer required [the infringing party] to use a particular type of equipment, the Government has not authorized or consented to any infringement of plaintiff's patent in the performance of the . . . contract." The court agreed: "In view of the general availability of noninfringing equipment, and the fact that use of equipment covered by plaintiff's patent was not required by the contract specifications or within instructions of the contracting officer, we find that the Government has not authorized or consented to any infringement of plaintiff's patent. . . . Under these circumstances, we cannot conclude that the mere inclusion of these [authorization and consent] provisions in the contract and the contractor's use of the allegedly infringing equipment, constitute sufficient evidence to establish the Government's authorization and consent. To hold otherwise would, in effect, mean that in every instance where the Government desires to avoid potential liability under Section 1498(a), it would be required to conduct a detailed and time-consuming investigation to determine whether the equipment the contractor selects for his own convenience infringes any outstanding patents."

The rule of <u>Carrier Corp</u>. has been acknowledged by subsequent cases:

"Even when the government expressly consents to infringement in order to perform a government contract, a government contractor's use of a patented device did not constitute authorization or consent where the choice of the device was the contractor's and where there was nothing in the contract that could not be performed without using the device. Carrier, 534 F.2d at 247-48. 'Implied government consent to infringement has been found only where particular government specifications required a particular patent infringement.' [citation omitted]. Yet the undisputed facts of the instant case demonstrated that there were myriad alternatives to plaintiffs' [infringing equipment]. Exhibits attached to defendant's motion illustrated sixteen different types of [equipment] that health care providers might have used in addition to plaintiffs'."

<u>Larson v. United States</u>, 26 Cl. Ct. 365, 370 (1992).

"48 CFR § 27.201-2(a) and 48 CFR § 52.227-1 provide . . . for inclusion of a narrower or 'limited' authorization and consent clause, based on the use of language which grants the Government's authorization and consent, but only where (i) the patented invention is embodied in the structure or composition of an article accepted by the Government, or (ii) the patented invention is used in tools or methods which necessarily results from compliance with specifications in the contract or specific written instructions from the contracting officer. . . . By choosing the scope of its consent in its selection of the contract language, the Government may control the extent of patent infringement it chooses to authorize, and the corresponding liability it chooses to accept. . . . However, where the Government limits its consent, as contemplated by use of language providing a narrower or 'limited' authorization and consent, that limited consent operates as a limited waiver of sovereign immunity and should be narrowly construed so as not to find consent and impose potential liability on the Government where the terms of the consent clause are not fully met. See Carrier Corp., 534 F.2d at 247 (finding no authorization or consent by the Government where the relevant contract included a limited authorization and consent clause, since non-infringing alternatives were available and no specification or written instructions required the use of any certain equipment). . . . Because § 1498 is an affirmative defense in suits between private parties, the burden is on the party asserting the defense to show the existence and extent of any Government authorization and consent, either express or implied. If a contractor establishes that the Government provided it with express or implied consent to infringe the patent, the contractor must then establish that its uses of the patented invention fall within the scope of that consent. Thus, when the Government provides the requisite authorization and consent, either express or implied, in relation to a Government contract or grant, the issue is 'which uses fall within the scope of the . . . grant and which uses are outside that scope.' "

<u>Madey v. Duke</u>, 413 F.Supp.2d 601, 608-10 (M.D.N.C. 2006).

In our case, Aeroflex bears the burden of proof to show th facts relating to its affirmative defense of authorization and consent; Ricoh is entitled to take discovery to show that Aeroflex may not rely on the defense because (among other things) the prime clauses are limited, because the federal government did not require the use of the infringing process, and that Aeroflex could have used a non-infringing process to designthe ASICs at issue. Thus, Aeroflex must produce a designee that can speak to all facts regarding the defense, including the six topics on which you currently refuse to present a designee. You are on notice that, if you refuse to present a designee on those topics, Ricoh reserves all its rights, including moving to strike the defense.

Regards, Ken

Ken Brothers
Dickstein Shapiro Morin & Oshinsky LLP
2101 L Street, N.W.
Washington DC 20037
phone (202) 429-2184
fax (202) 887-0689

New contact information as of July 10, 2006:
Dickstein Shapiro LLP
1825 Eye Street NW
Washington DC 20006
direct (202) 420-4128
phone (202) 420-2200
fax (202) 420-2201

EXHIBIT 3

FOR IMMEDIATE RELEASE: March 27, 2000

CONTACT:

Teresa Farris
UTMC Microelectronic Systems Inc. (UTMC)
4350 Centennial Blvd.
Colorado Springs, CO 80907
719-594-8035 (voice)
719-594-8468 (fax)
Email: farris@utmc.aeroflex.com

UTMC INTRODUCES STRATEGIC RadHard™
0.6 micron GATE ARRAY FAMILY

Colorado Springs, CO –UTMC Microelectronic Systems Inc. (UTMC), an Aeroflex company, (NASDAQ:ARXX) announces their Strategic RadHard™ gate array family called the UT0.6µSRH. The UT0.6µSRH is designed specifically for high reliability space applications that require high SEU immunity and over 1 Mega rad of total dose hardness. The UT0.6µSRH is fabricated in a commercial 0.6u silicon gate CMOS process that utilizes a special process module run in AMI's commercial foundry. This process enhances the total dose radiation hardness of the field and gate oxides while maintaining circuit density, reliability, and commercial silicon performance.

According to Peter Milliken, ASIC Product Line Manager, "This product release represents an industry breakthrough. It is the first product that is fabricated in a commercial fab, that is SEL immune and is guaranteed to have a hardness of at least 1 Mega rads. The introduction of radiation-hardened products from a commercial fab is significant because it allows commercial and military space products to take advantage of the rapid advances in commercial silicon technology."

"The UT0.6µSRH follows UTMC's successful UT0.6µCRH Commercial RadHard™ process," continued Milliken. "UTMC was the first to introduce a process guaranteed to 300K rads(Si) produced on a commercial fab. Customers have incorporated the UT0.6µCRH Commercial RadHard™ gate arrays into their products and UTMC has listened to their requests for a 1 Mega Rad product. This will save customers development time and reduce costs."

UTMC's UT0.6µSRH gate array family features array sizes up to 600,000 usable gates and is ISO 9001 and QML Class Q and V compliant. The gate array family is radiation hardened to 1 Mega Rad and can meet SEU immunity to less than 1.0E-10 errors/bit-day. It features clock rates up to 215MHz and operating voltage of 5V and 3.3V.

The UT0.6uSRH family of gate arrays is supported by Mentor Graphics and Synopsys design platforms in VHDL and Verilog design languages on HP, NT and Sun workstations. A robust cell library with over 170 options include SSI, MSI, and 54XX equivalent functions, as well as configurable RAM, MIL-STD-1553 functions, microcontrollers, and other macro/megafunctions.

UTMC, an Aeroflex company, (NASDAQ:ARXX) is a supplier of semicustom and standard VLSI circuits and custom circuit card assemblies and is dedicated to the aerospace and defense marketplace. UTMC has received Qualified Manufacturer List (QML) certification for Class T, Class Q and Class V and ISO 9002 Registration from Underwriters Laboratory. Additionally, UTMC has received a letter of compliance for ISO 9001 from the Defense Supply Center Columbus.

###

For a copy of the UT0.6µSRH datasheet, call 1-800-645-UTMC, write UTMC, 4350 Centennial Blvd., Colorado Springs, CO 80907, or visit UTMC's home page at www.utmc.com.

EXHIBIT 4

Semicustom Products

UT0.6μCRH/SRH Commercial RadHard™ and Strategic RadHard™ Gate Array Family

Data Sheet
December 2003

AEROFLEX
A passion for performance.

FEATURES

- ❑ Multiple gate array sizes up to 600,000 usable equivalent gates
- ❑ Toggle rates up to 150 MHz
- ❑ Advanced 0.6μ (0.5μL_{eff}) radiation-tolerant silicon gate CMOS processed in a commercial fab
- ❑ Operating voltage of 5V and/or 3.3V
- ❑ QML Class Q & V compliant
- ❑ Designed specifically for high reliability applications
- ❑ Commercial RadHard™ for radiation-tolerant to 300K rads to meet space requirements and SEU-immune to less than 2.0E-10 errors/bit-day
- ❑ Strategic RadHard™ for radiation environments to 1 Mega rads to meet space requirements and SEU-immune to less than 2.0E-10 errors/bit-day
- ❑ JTAG (IEEE 1149.1) boundary-scan supported
- ❑ Low noise package technology for high speed circuits
- ❑ Design support using Mentor Graphics® and Synopsys™ in VHDL or Verilog design languages on Sun® and Linux workstations
- ❑ Supports cold sparing for power down applications
- ❑ Supports voltage translation
  - 5V bus to 3.3V bus
  - 3.3V bus to 5V bus

PRODUCT DESCRIPTION

The high-performance UT0.6μCRH/SRH gate array family features densities up to 600,000 equivalent gates and is available in MIL-PRF-38535 QML Q and V product assurance levels and is radiation-tolerant.

The Commercial RadHard™ and Strategic RadHard™ silicon is fabricated at American Microsystems Incorporated (AMI) using a minimally invasive processing module, developed by UTMC, that enhances the total dose radiation hardness of the field and gate oxides while maintaining circuit density and reliability. In addition, for both greater transient radiation-hardness and latchup immunity, the UTMC 0.6μ process is built on epitaxial substrate wafers.

Developed using UTMC's patented architectures, the UT0.6μCRH/SRH gate array family uses a highly efficient continuous column transistor architecture for the internal cell construction. Combined with state-of-the-art placement and routing tools, the utilization of available transistors is maximized using three levels of metal interconnect.

The UT0.6μCRH/SRH family of gate arrays is supported by an extensive cell library that includes SSI, MSI, and 54XX equivalent functions, as well as configurable RAM and cores. UTMC's core library includes the following functions:

- Intel 80C31® equivalent
- Intel 80C196® equivalent
- MIL-STD-1553 functions (BRCTM, RTI, RTMP)
- MIL-STD-1750 microprocessor
- RISC microcontroller
- Configurable RAM (SRAM, DPSRAM)
- USART (82C51)
- EDAC

Table 1. Gate Densities

DEVICE PART NUMBERS	EQUIVALENT USABLE GATES[1]	SIGNAL I/O[2]	POWER & GROUND PADS[3]
UT06MRA010	10,000	192	48
UT06MRA025	25,000	192	48
UT06MRA050	50,000	192	48
UT06MRA075	75,000	432	96
UT06MRA100	100,000	432	96
UT06MRA150	150,000	432	96
UT06MRA200	200,000	432	96
UT06MRA250	250,000	432	96
UT06MRA300	300,000	432	96
UT06MRA350	350,000	432	96
UT06MRA400	400,000	544	144
UT06MRA450	450,000	544	144
UT06MRA500	500,000	544	144
UT06MRA550	550,000	544	144
UT06MRA600	600,000	544	144

Notes:
1. Based on NAND2 equivalents. Actual usable gate count is design-dependent. Estimates reflect a mix of functions including RAM.
2. Includes five pins that may or may not be reserved for JTAG boundary-scan, depending on user requirements.
3. Reserved for dedicated V_{DD}/V_{SS} and V_{DDQ}/V_{SSQ}.
4. Aeroflex offers three die sizes: KD (280 mils), KB (525 mils), and KM (677 mils).

Low-noise Device and Package Solutions

The UT0.6μCRH/SRH array family's output drivers feature programmable slew rate control for minimizing noise and switching transients. This feature allows the user to optimize edge characteristics to match system requirements. Separate on-chip power and ground buses are provided for internal cells and output drivers which further isolate internal design circuitry from switching noise.

In addition, Aeroflex UTMC offers advanced low-noise package technology with multi-layer, co-fired ceramic construction featuring built-in isolated power and ground planes (see Table 2). These planes provide lower overall resistance/inductance through power and ground paths which minimize voltage drops during periods of heavy switching. These isolated planes also help sustain supply voltage during dose rate events, thus preventing rail span collapse.

Flatpacks are available with up to 352 leads; PGAs are available with up to 299 pins and LGAs to 472 pins. Aeroflex UTMC's flatpacks feature a non-conductive tie bar that helps maintain lead integrity through test and handling operations. In addition to the packages listed in Table 2, Aeroflex UTMC offers custom package development and package tooling modification services for individual requirements.

Table 2. Packages

PACKAGE TYPE/ LEADCOUNT[1]	025	050	075	100	150	200	250	300	350	400	450	500	550	600
Flatpack														
84	X	X												
132	X	X												
172	X	X												
196	X	X												
256			X	X	X	X	X	X	X	X	X	X	X	X
304			X	X	X	X	X	X	X					
352										X	X	X	X	X
PGA[2]														
299						X	X	X	X					
LGA														
472										X	X	X	X	X

Notes:
1. The number of device I/O pads available may be restricted by the selected package.
2. PGA packages have one additional non-connected index pin (i.e., 84 + 1 index pin = 85 total package pins for the 85 PGA).
   Contact Aeroflex UTMC for specific package drawings.

Extensive Cell Library

The UT0.6μCRH/SRH family of gate arrays is supported by an extensive cell library that includes SSI, MSI, and 54XX-equivalent functions, as well as RAM and other library functions. User-selectable options for cell configurations include scan for all register elements, as well as output drive strength. Aeroflex UTMC's core library includes the following functions:

- Intel® 80C31 equivalent
- Intel® 80C196 equivalent
- MIL-STD-1553 functions (BCRTM, RTI, RTMP)
- MIL-STD-1750 microprocessor
- Standard microprocessor peripheral functions
- Configurable RAM (SRAM, DPsRAM)
- RISC Microcontroller
- USART (82C51)
- EDAC

Refer to Aeroflex UTMC's UT0.6μCRH/SRH Design Manual for complete cell listing and details.

I/O Buffers

The UT0.6μCRH/SRH gate array family offers up to 544 signal I/O locations (note: device signal I/O availability is affected by package selection and pinout.) The I/O cells can be configured by the user to serve as input, output, bidirectional, three-state, or additional power and ground pads. Output drive options range from 2 to 12mA. To drive larger off-chip loads, output drivers may be combined in parallel to provide additional drive up to 24mA.

Other I/O buffer features and options include:

- Slew rate control
- Pull-up and pull-down resistors
- TTL, CMOS, and Schmitt levels
- Cold sparing
- Voltage translation
  - 5V bus to 3.3V bus
  - 3.3V bus to 5V bus

JTAG Boundary-Scan

The UT0.6μCRH/SRH arrays provide for a test access port and boundary-scan that conforms to the IEEE Standard 1149.1 (JTAG). Some of the benefits of this capability are:

- Easy test of complex assembled printed circuit boards
- Gain access to and control of internal scan paths
- Initiation of Built-In Self Test

Clock Driver Distribution

Aeroflex UTMC design tools provide methods for balanced clock distribution that maximize drive capability and minimize relative clock skew between clocked devices.

Speed and Performance

Aeroflex UTMC specializes in high-performance circuits designed to operate in harsh military and radiation environments. Table 3 presents a sampling of typical cell delays.

Note that the propagation delay for a CMOS device is a function of its fanout loading, input slew, supply voltage, operating temperature, and processing radiation tolerance. In a radiation environment, additional performance variances must be considered. The UT0.6μCRH/SRH array family simulation models account for all of these effects to accurately determine circuit performance for its particular set of use conditions.

Power Dissipation

Each internal gate or I/O driver has an average power consumption based on its switching frequency and capacitive loading. Radiation-tolerant processes exhibit power dissipation that is typical of CMOS processes. For a rigorous power estimating methodology, refer to the Aeroflex UTMC UT0.6μCRH/SRH Design Manual or consult with a Aeroflex UTMC Applications Engineer.

Typical Power Dissipation

1.1μW/Gate-MHz@5.0V	0.4μW/Gate-MHz@3.3V

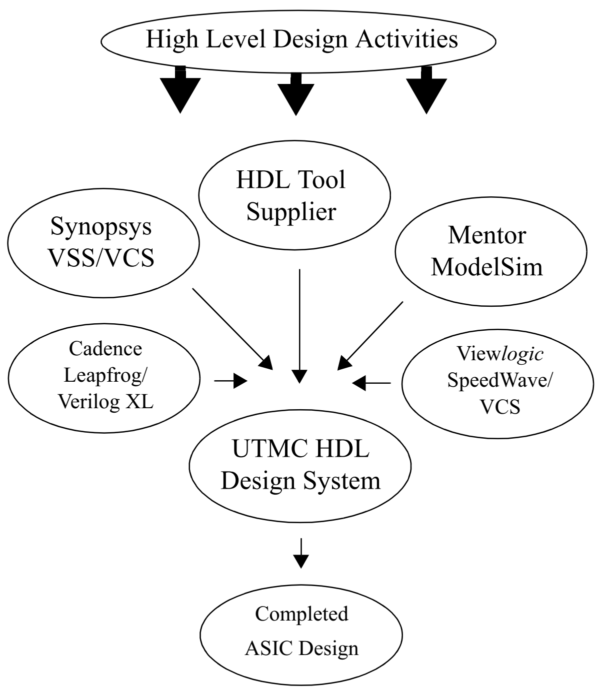
ASIC DESIGN SOFTWARE

Using a combination of state-of-the-art third-party and proprietary design tools, Aeroflex UTMC delivers the CAE support and capability to handle complex, high-performance ASIC designs from design concept through design verification and test.

Aeroflex UTMC's flexible circuit creation methodology supports high level design by providing UT0.6μCRH/SRH libraries for Mentor Graphics and Synopsys synthesis tools. Design verification is performed in any VHDL or Verilog simulator or the Mentor Graphics environment, using Aeroflex UTMC's robust libraries. Aeroflex UTMC also supports Automatic Test Program Generation to improve design testing.

Aeroflex UTMC HDL DESIGN SYSTEMS

Aeroflex UTMC offers a Hardware Description Language (HDL) design system supporting VHDL and Verilog. Both the VHDL and Verilog libraries provide sign-off quality models and robust tools.



Aeroflex UTMC HDL Design Flow

The VHDL libraries are VITAL 3.0 compliant, and the Verilog libraries are OVI 1.0 compliant.With the library capabilities Aeroflex UTMC provides, you can use High Level Design methods to synthesize your design for simulation. Aeroflex UTMC also provides tools to verify that your HDL design will result in working ASIC devices.

Either of Aeroflex UTMC's HDL design system lets you easily access Aeroflex UTMC's RadHard capabilities.

ADVANTAGES OF THE AEROFLEX UTMC HDL DESIGN SYSTEMS

- The Aeroflex UTMC HDL Design System gives you the freedom to use tools from Synopsys, Mentor Graphics, Cadence, View*logic*, and other vendors to help you synthesize and verify a design.
- Aeroflex UTMC's Logic Rules Checker and Tester Rules Checker allow you to verify partial or complete designs for compliance with Aeroflex UTMC design rules.
- Aeroflex UTMC HDL Design System accepts back-annotation of timing information through SDF.
- Your design stays entirely within the language in which you started (VHDL or Verilog) preventing conversion headaches.

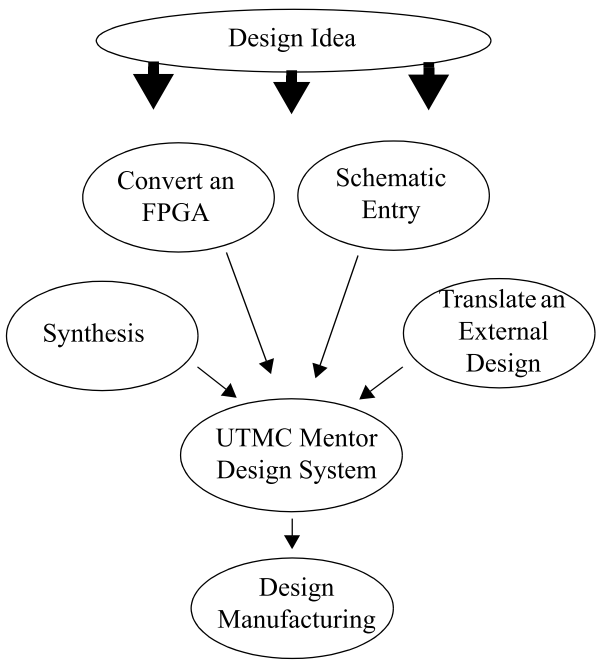
XDT^{sm} (eXternal Design Translation)

Through Aeroflex UTMC's XDT services, customers can convert an existing non-Aeroflex UTMC design to Aeroflex UTMC's processes. The XDT tool is particularly useful for converting an FPGA to a Aeroflex UTMC radiation-tolerant gate array. The XDT translation tools convert industry standard netlist formats and vendor libraries to Aeroflex UTMC formats and libraries. Industry standard netlist formats supported by Aeroflex UTMC include:

- VHDL
- Verilog HDL^{TM}
- FPGA source files (Actel, Altera, Xilinx)
- EDIF
- Third-party netlists supported by Synopsys

AEROFLEX UTMC MENTOR GRAPHICS DESIGN SYSTEM

The Aeroflex UTMC Mentor Graphics Design System software is fully integrated into the Mentor Graphics design environment, making it familiar and easy to use. Aeroflex UTMC tools support Mentor functions such as cross-highlighting, graphical menus, and design navigation.



Aeroflex UTMC Mentor Graphics Design

After creating a design in the Mentor Graphics environment, you can easily verify the design for electrical rules compliance with the Aeroflex UTMC Logic Rules Checker. Testability can be verified with the Aeroflex UTMC Tester Rules Checker. Both of these tools are fully integrated into the Mentor Graphics Environment.

When you have completed all design activities, Aeroflex UTMC's Design Transfer tool captures all the required files and prepares them for easy transfer to Aeroflex UTMC. Aeroflex UTMC uses this data to convert your design into a packaged and tested device.

ADVANTAGES OF THE AEROFLEX UTMC MENTOR DESIGN SYSTEM

- Aeroflex UTMC customers have successfully used the Aeroflex UTMC Mentor Graphics Design System for over a decade.
- Aeroflex UTMC's Logic and Tester Rules Checker tools allow you to verify partial or complete designs for compliance with Aeroflex UTMC manufacturing practices and procedures.
- The Design System accepts pre-and post-layout timing information to ensure your design results in devices that meet your specifications.
- The Design System supports Leonardo, and database transfer between Synopsys and Mentor.
- The Design System supports powerful Mentor Graphics ATPG capabilities.

TOOLS SUPPORTED BY AEROFLEX UTMC

Aeroflex UTMC supports libraries for:

- Mentor Graphics
- ModelSim
- Synopsys
- Design Compiler
- PrimeTime
- Formality
- TetraMax
- VITAL-compliant VHDL Tools
- OVI-compliant Verilog Tools

TRAINING AND SUPPORT

Aeroflex UTMC personnel conduct training classes tailored to meet individual needs. These classes can address a wide mix of engineering backgrounds and specific customer concerns. Applications assistance is also available through all phases of ASIC Design.

Table 3. Typical Cell Delays

CELL	OUTPUT TRANSITION	PROPAGATION DELAY [1]	
Internal Gates		$V_{DD} = 5.0V$	$V_{DD} = 3.3V$
INV1, Inverter	HL	.15	.16
	LH	.23	.29
INV4, Inverter 4X	HL	.06	.07
	LH	.10	.16
NAND2, 2-Input NAND	HL	.19	.25
	LH	.22	.33
NOR2, 2-Input NOR	HL	.16	.22
	LH	.32	.45
DFF - CLK to Q	HL	.81	1.12
	LH	.76	1.06
	HL	.75	1.05
	LH	.61	.85
Output Buffers			
OC5050N4, CMOS	HL	3.85	2.15
	LH	4.66	3.76
OT5050N4, TTL, 4mA	HL	5.58	5.49
	LH	2.52	2.93
OT5050N12, TTL, 12mA	HL	2.42	
	LH	1.29	
Input Buffers			
IC5050, CMOS	HL	.81	1.07
	LH	1.16	1.18
IT5050, TTL	HL	1.39	1.12
	LH	1.16	1.30

Note:
1. All specifications in ns (typical). Output load capacitance is 50pF. Fanout loading for input buffers and gates is the equivalent of two gate input loads.

PHYSICAL DESIGN

Using three layers of metal interconnect, Aeroflex UTMC achieves optimized layouts that maximize speed of critical nets, overall chip performance, and design density up to 600,000 equivalent gates.

Test Capability

Aeroflex UTMC supports all phases of test development from test stimulus generation through high-speed production test. This support includes ATPG, fault simulation, and fault grading. Scan design options are available on all UT0.6μCRH/SRH storage elements. Automatic test program development capabilities handle large vector sets for use with Aeroflex UTMC's LTX/Trillium MicroMasters, supporting high-speed testing (up to 80MHz with pin multiplexing).

Unparalleled Quality and Reliability

Aeroflex UTMC is dedicated to meeting the stringent performance requirements of aerospace and defense systems suppliers. Aeroflex UTMC maintains the highest level of quality and reliability through our Quality Management Program under MIL-PRF-38535 and ISO-9001. In 1988, we were the first gate array manufacturer to achieve QPL certification and qualification of our technology families. Our product assurance program has kept pace with the demands of certification and qualification.

Our quality management plan includes the following activities and initiatives.

- Quality improvement plan
- Failure analysis program
- SPC plan
- Corrective action plan
- Change control program
- Standard Evaluation Circuit (SEC) and Technology Characterization Vehicle (TCV) assessment program
- Certification and qualification program

Because of numerous product variations permitted with customer specific designs, much of the reliability testing is performed using a Standard Evaluation Circuit (SEC) and Technology Characterization Vehicle (TCV). The TCV utilizes test structures to evaluate hot carrier aging, electromigration, and time dependent test samples for reliability testing. Data from the wafer-level testing can provide rapid feedback to the fabrication process, as well as establish the reliability performance of the product before it is packaged and shipped.

Radiation Tolerance

Aeroflex UTMC incorporates radiation-tolerance techniques in process design, design rules, array design, power distribution, and library element design. All key radiation-tolerance process parameters are controlled and monitored using statistical methods and in-line testing.

PARAMETER	RADIATION TOLERANCE	NOTES
Total dose	1.0E5 rad(SiO_2) 3.0E5 rad(SiO_2)	1 2
Dose rate upset	1.0E8 rad(Si)/sec	3
Dose rate survivability	1.0E11 rad(Si)/sec	4
SEU	<2.0E-10 errors per cell-day	4, 5
Projected neutron fluence	1.0E14 n/sq cm	
Latchup	Latchup-immune over specified use conditions	

Notes:
1. Total dose Co-60 testing is in accordance with MIL-STD-883, Method 1019. Data sheet electrical characteristics guaranteed to 1.0E5 rads(SiO_2). All post-radiation values measured at 25°C.
2. Total dose Co-60 testing is in accordance with MIL-STD-883, Method 1019 at dose rates <1 rad(SiO_2)/s.
3. Short pulse 20ns FWHM (full width, half maximum).
4. Is design dependent; SEU limit based on standard evaluation circuit at 4.5V worst case condition.
5. SEU-hard flip-flop cell. Non-hard flip-flop typical is 4E-8.

ABSOLUTE MAXIMUM RATINGS [1]
(Referenced to V_{SS})

SYMBOL	PARAMETER	LIMITS
V_{DD}	DC supply voltage	-0.3 to 6.0V
$V_{I/O}$	Voltage on any pin	-0.3V to V_{DD} + 0.3
T_{STG}	Storage temperature	-65 to +150°C
T_J	Maximum junction temperature	+175°C
I_{LU}	Latchup immunity	±150mA
I_I	DC input current	±10mA
T_{LS}	Lead temperature (soldering 5 sec)	+300°C

Note:
1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS
V_{DD}	Positive supply voltage	3.0 to 5.5V
T_C	Case temperature range	-55 to +125C
V_{IN}	DC input voltage	0V to V_{DD}

DC ELECTRICAL CHARACTERISTICS
(V_{DD} = 5.0V ±10%; -55°C < T_C < +125°C)

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage [1] TTL inputs CMOS	V_{DD} = 4.5V and 5.5V			0.8 .3V_{DD}	V
V_{IH}	High-level input voltage [1] TTL inputs CMOS	V_{DD} = 4.5V and 5.5V	2.2 .7V_{DD}			V
V_{T+}	Schmitt Trigger, positive going [1] threshold	V_{DD} = 4.5V and 5.5V			.7V_{DD}	V
V_{T-}	Schmitt Trigger, negative going [1] threshold	V_{DD} = 4.5V and 5.5V	.3V_{DD}			V
V_H	Schmitt Trigger, typical range of hysteresis [2]		0.6			V
I_{IN}	Input leakage current TTL, CMOS, and Schmitt inputs Inputs with pull-down resistors Inputs with pull-down resistors Inputs with pull-up resistors Inputs with pull-up resistors Cold Spare Inputs - Normal Mode Cold Spare Inputs - Cold Spare Mode	V_{DD} = 5.5V V_{IN} = V_{DD} and V_{SS} V_{IN} = V_{DD} V_{IN} = V_{SS} V_{IN} = V_{SS} V_{IN} = V_{DD} V_{IN} = 0 to 5.5V V_{DD} = V_{SS} = 0V V_{IN} = V and 5.5V	-1 +20 -5 -225 -5 -5 -5		1 +225 +5 -20 +5 +5 +5	µA
V_{OL}	Low-level output voltage[3] TTL 2.0mA buffer TTL 4.0mA buffer TTL 8.0mA buffer TTL 12.0mA buffer * CMOS outputs CMOS outputs (optional) CMOS outputs (cold spare)	V_{DD} = 4.5V I_{OL} = 2.0mA I_{OL} = 4.0mA I_{OL} = 8.0mA I_{OL} = 12.0mA I_{OL} = 1.0µA I_{OL} = 100µA I_{OL} = 100µA			0.4 0.4 0.4 0.4 0.05 0.25 0.25	V
V_{OH}	High-level output voltage[3] TTL 2.0mA buffer TTL 4.0mA buffer TTL 8.0mA buffer TTL 12.0mA buffer * CMOS outputs CMOS outputs (optional) CMOS outputs (cold spare)	V_{DD} = 4.5V I_{OH} = -2.0mA I_{OH} = -4.0mA I_{OH} = -8.0mA I_{OH} = -12.0mA I_{OH} = -1.0µA I_{OH} = -100µA I_{OH} = -100µA	2.4 2.4 2.4 2.4 V_{DD}-0.05 V_{DD}-0.35 V_{DD}-0.35			V

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
I_{OZ}	Three-state output leakage current TTL 2.0mA buffer TTL 4.0mA buffer, CMOS TTL 8.0mA buffer TTL 12.0mA buffer * Cold Spare Inputs - normal mode Cold Spare Inputs - cold spare mode	V_{DD} = 5.5V V_O = 0V and 5.5V $V_{DD} = V_{SS} = 0$ V_{DD} = 0 to 5.5V	 -5 -10 -20 -30 -5 -5		 5 10 20 30 -5 -5	µA
I_{OS}	Short-circuit output current [2,4] TTL 2.0mA buffer TTL 4.0mA buffer, CMOS TTL 8.0mA buffer TTL 12.0mA buffer *	V_O = 0V and 5.5V	 -50 -100 -200 -300		 50 100 200 300	mA
I_{DDQ}	Quiescent Supply Current[6] Group A subgroups 1,3	V_{DD} = 5.5V 200K gates 400K gates 600K gates			 50 100 180	µA
	Group A subgroup 2	V_{DD} = 5.5V 200K gates 400K gates 600K gates			 1 2 3	mA
	Group A, subgroup 1 RHA Designator: M, D, P, L, R	V_{DD} = 5.5V 200K gates 400K gates 600K gates			 4 8 12	mA

Notes:

* Contact Aeroflex UTMC prior to usage.

1. Functional tests are conducted in accordance with MIL-STD-883 with the following input test conditions: $V_{IH} = V_{IH}(min) + 20\%, - 0\%$; $V_{IL} = V_{IL}(max) + 0\%, - 50\%$, as specified herein, for TTL, CMOS, or Schmitt compatible inputs. Devices may be tested using any input voltage within the above specified range, but are guaranteed to $V_{IH}(min)$ and $V_{IL}(max)$.
2. Supplied as a design limit but not guaranteed or tested.
3. Per MIL-PRF-38535, for current density $\leq$5.0E5 amps/cm^2, the maximum product of load capacitance (per output buffer) times frequency should not exceed 3,765pF*MHz.
4. Not more than one output may be shorted at a time for maximum duration of one second.
5. Capacitance measured for initial qualification and when design changes may affect the value. Capacitance is measured between the designated terminal and V_{SS} at frequency of 1MHz @0V and a signal amplitude of $\leq$50mV RMS.
6. All inputs with internal pull-ups should be left floating. All other inputs should be tied high or low.

DC ELECTRICAL CHARACTERISTICS
(V_{DD} = 3.3V $\pm$.3V; -55°C < T_C < +125°C)

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage [1] CMOS	V_{DD} = 3.0V and 3.6V			.3V_{DD}	V
V_{IH}	High-level input voltage [1] CMOS	V_{DD} = 3.0V and 3.6V	.7V_{DD}			V
V_T+	Schmitt Trigger, positive going [1] threshold	V_{DD} = 3.0V and 3.6V			.7V_{DD}	V
V_T-	Schmitt Trigger, negative going [1] threshold	V_{DD} = 3.0V and 3.6V	.3V_{DD}			V
V_H	Schmitt Trigger, typical range of hysteresis [2]		.6			V
I_{IN}	Input leakage current TTL, CMOS, and Schmitt inputs Inputs with pull-down resistors Inputs with pull-down resistors Inputs with pull-up resistors Inputs with pull-up resistors Cold Spare Inputs - normal mode Cold Spare Inputs - cold spare mode	V_{DD} = 3.6V V_{IN} = V_{DD} and V_{SS} V_{IN} = V_{DD} V_{IN} = V_{SS} V_{IN} = V_{SS} V_{IN} = V_{DD} V_{IN} = 0 to 3.6V V_{DD} = V_{SS} = 0V V_{IN} = V and 3.6V	 -1 +10 -5 -225 -5 -5 -5		 1 +225 +5 -10 +5 +5 +5	µA
V_{OL}	Low-level output voltage CMOS outputs CMOS outputs (optional) CMOS outputs (cold spare)	 I_{OL} = 1.0µA I_{OL} = 100µA I_{OL} = 100µA			 0.05 0.25 0.25	V
V_{OH}	High-level output voltage CMOS outputs CMOS outputs (optional) CMOS outputs (cold spare)	 I_{OH} = -1.0µA I_{OH} = -100µA I_{OH} = -100µA	 V_{DD}-0.05 V_{DD}-0.35 V_{DD}-0.35			V

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
I_{OZ}	Three-state output leakage current CMOS	$V_{DD} = 3.6V$	-20		20	μA
	Cold Spare Inputs - normal mode	$V_O = V_{DD}$ and V_{SS}	-5		5	
	Cold Spare Inputs - cold spare mode	$V_{DD} = V_{SS} = 0V$ $V_O = 0V$ and $3.6V$	-5		5	
I_{OS}	Short-circuit output current [2,4] CMOS	$V_O = V_{DD}$ and V_{SS}	-200		200	mA
I_{DDQ}	Quiescent Supply Current[6] Group A subgroups 1,3	$V_{DD} = 5.5V$ 200K gates 400K gates 600K gates			50 100 180	μA
	Group A subgroup 2	$V_{DD} = 5.5V$ 200K gates 400K gates 600K gates			1 2 3	mA
	Group A, subgroup 1 RHA designator: M, D, P, L, R	$V_{DD} = 5.5V$ 200K gates 400K gates 600K gates			4 8 12	mA
C_{IN}	Input capacitance [5]			17		pF
C_{OUT}	Output capacitance [5] CMOS			18		pF
C_{IO}	Bidirect I/O capacitance [5] CMOS			19		pF

Notes:

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1. Functional tests are conducted in accordance with MIL-STD-883 with the following input test conditions: $V_{IH} = V_{IH}(min) + 20\%, - 0\%$; $V_{IL} = V_{IL}(max) + 0\%, - 50\%$, as specified herein, for TTL, CMOS, or Schmitt compatible inputs. Devices may be tested using any input voltage within the above specified range, but are guaranteed to $V_{IH}(min)$ and $V_{IL}(max)$.
2. Supplied as a design limit but not guaranteed or tested.
3. Per MIL-PRF-38535, for current density $\leq 5.0E5$ amps/cm^2, the maximum product of load capacitance (per output buffer) times frequency should not exceed 3,765pF*MHz.
4. Not more than one output may be shorted at a time for maximum duration of one second.
5. Capacitance measured for initial qualification and when design changes may affect the value. Capacitance is measured between the designated terminal and V_{SS} at frequency of 1MHz @0V and a signal amplitude of ≤50mV RMS.
6. All inputs with internal pull-ups should be left floating. All other inputs should be tied high or low.

Notes

COLORADO
Toll Free: 800-645-8862
Fax: 719-594-8468

INTERNATIONAL
Tel: 805-778-9229
Fax: 805-778-1980

NORTHEAST
Tel: 603-888-3975
Fax: 603-888-4585

SE AND MID-ATLANTIC
Tel: 321-951-4164
Fax: 321-951-4254

WEST COAST
Tel: 949-362-2260
Fax: 949-362-2266

CENTRAL
Tel: 719-594-8017
Fax: 719-594-8468

www.aeroflex.com info-ams@aeroflex.com

AEROFLEX
A passion for performance.

Our passion for performance is defined by three attributes represented by these three icons: solution-minded, performance-driven and customer-focused